1. (Amended) A semiconductor device having a multiple layer wiring structure that is provided with two or more metal layers and having a stack VIA portion in which, when connecting in a connection area a connection metal layer and a layer to be connected that is removed from the connection metal layer with one or more intermediate metal layers, wherein

the semiconductor device having a multiple layer wiring structure comprises:

two or more partitioned intermediate metal layers that are partitioned inside the connection area; and

an intermediate metal layer wiring area that is sandwiched by the partitioned intermediate metal layers.

2. (Amended) The semiconductor device according to claim 1, wherein the connection metal layer and the layer to be connected intersect in a connection area.

Add new claims 19-21 as follows:

~~19.~~ 11 (Added) A semiconductor device having a multiple layer wiring and a stack VIA, comprising:

a connection metal layer;

a layer to be connected with the connection metal layer; and

one or more intermediate layers, provided between the connection metal layer and the layer to be connected, partitioned into two or more partitioned intermediate layers,

30

a

wherein the partitioned intermediate layers comprise:

at least one intermediate metal layer having a stack VIA; and

at least one intermediate metal layer wiring area where a wire can be passed through.

12
20. (Added) A semiconductor device having a multiple layer wiring and a stack VIA, wherein the semiconductor device is generated by the method provided with an automatic wiring design program for performing wiring design automatically using the wiring method, the wiring method comprising:

a step of determining a connection metal layer and a layer to be connected with the connection metal layer that is removed from the connection metal layer with one or more intermediate metal layers;

a step of connecting the connection metal layer and the layer to be connected via a partitioned intermediate metal layer having a stack VIA,

wherein the one or more intermediate layers are partitioned into at least one partitioned intermediate metal layer and at least one intermediate metal layer wiring area.

13
21. (Added) A semiconductor device having a multiple layer wiring and a stack VIA, wherein the semiconductor device is generated by the method provided with an automatically wiring design program for performing wiring design automatically using the wiring method, and when connecting in a connection area a connection metal layer and a layer to be connected that is removed from the connection metal layer with one or more intermediate metal layers, the intermediate metal

A2 cont'd.

layers are partitioned within the connection area, and an area sandwiched by the partitioned intermediate metal layers is formed as an intermediate metal layer wiring area.